REMARKS

Claims 1-20 remain pending in this application.

With respect to claim 5, the Examiner states: "[I]t suggests to add the legend of k cited in the claim as it appears in the claim first time." The Examiner's objection and the corrective action required by the Examiner are unclear. The Applicants respectfully request further clarification as to the precise nature of the Examiner's objection to the claim language and the correction requested by the Examiner. The Applicants submit that claim 5 is definite in view of the description in the specification. However, the Applicants are receptive to considering other alternative language that may be amenable to the Examiner.

The Examiner rejected claims 1-2 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,621,857 (***Belotserkovsky***). Claim 1, in part, calls for receiving a first signal having a first data rate and determining, based at least on the first signal, a second signal having a second data rate, wherein the second data rate is lower than the first data rate. Thus, claim 1 calls for the data rate of the second signal to be lower than the data rate of the first signal. The Examiner asserts that the input to the element 402 corresponds to the "first signal," and that the output of the element 402 corresponds to the "second signal." Even under the Examiner's application of ***Belotserkovsky*** to claim1, the Applicants assert that ***Belotserkovsky*** at least fails to teach a second signal that has a lower data rate than the first signal. In fact, the description in ***Belotserkovsky*** contradicts the position taken by Examiner. As an initial matter, Figure 5 of ***Belotserkovsky*** makes it abundantly clear that the signals to the left of the dashed line operate at the "chip rate," while the signals to the right of the dashed line operate at the "symbol rate." *See* bottom of Figure 5, which shows arrows indicating the respective data rates. The description of

Figure 5 further hammers this point. In particular, at col. 7, lines 12-17, ***Belotserkovsky*** states that all the signal processing to the left of the dashed line occurs at a chip rate, while the signaling processing to the right of the dashed line occurs at the symbol rate. The ***Belotserkovsky*** reference goes further and clarifies that the components to the left of the dashed line (such as the filter 432, NCO 433, element 402, element 403) operate at the chip rate, while the components to the right of the dashed line (such as circuit 431) operate at the symbol rate. See col. 7, line 25-27 of ***Belotserkovsky***. Put another way, ***Belotserkovsky*** expressly teaches that the "data rate" of the signals to the left of the dashed line is the same, including the data rate of the signal that is input to the element 402 and the data rate of the signal that is output from the element 402. In fact, Figure 7 further clarifies this point, as it shows the rate of the "samples" (which correspond to the output of element 402) to be at the chip rate, and then shows the rate of the "symbols" (which corresponds to the output of element 404) to be at a symbol rate. Thus, contrary to the Examiner's assertion, ***Belotserkovsky*** at least does not teach that the data rate of the output signal (the second signal) of the element 402 is lower than the data rate of the input signal (the first signal) to the element 402. The Examiner apparently confuses the "sampling rate" of the signals with the actual "data rate" of the signals. While ***Belotserkovsky*** may indicate that the input to the element 402 is sampled at a 2x chip rate, it does not teach that the data rate of the second signal is lower than that of the first signal. To the contrary, for reasons discussed above, ***Belotserkovsky*** teaches that the two rates are, in fact, the same.

For at least this reason, claims 1 and 2 are allowable. Additionally, because the Examiner relies on ***Belotserkovsky*** to reject the other pending claims, these other claims are also allowable in view of at least this deficiency in ***Belotserkovsky***.

The Examiner rejects other pending claims under 35 U.S.C. § 103(a) as being unpatentable over ***Belotserkovsky*** and further in view of various other references. Applicants respectfully traverse this rejection. The criteria for establishing a *prima facie* case of obviousness has been previously stated by the Applicants, and thus is not repeated herein. The Examiner appears to use the pending claims as a template to combine the prior art references to make a rejection under 35 U.S.C. §103. The fact that the Examiner relies on no less than four different references to reject the claims is a clear indication of the weakness in the Examiner's position. The Applicants dispute the appropriateness of combining these references and contend that the Examiner has failed to provide the requisite suggestion or motivation to combine the references in the manner claimed.

Thus, in light of the arguments presented above, Applicants respectfully assert that the pending claims are allowable. Accordingly, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4064 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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